B. AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A circuit for testing serial ports in an automatic test system, comprising:

a receiver having an input and an output, for receiving a test signal from a transmit line of a serial port;

a time measurement circuit, coupled to the output of the receiver, for measuring timing characteristics of test signals received by the receiver;

a transmitter having an input and an output, for transmitting a test signal to a receive line of the serial port, wherein the input of the transmitter is coupled to the output of the receiver for establishing a loopback connection; and

a parametric measurement circuit, coupled to the input of the receiver, for evaluating steady-state characteristics of the transmit line of the serial port.

2. (Previously Presented) A circuit as recited in claim 1, wherein the parametric measurement circuit is further coupled to the output of the transmitter, for evaluating steady-state characteristics of the receive line of the serial port.

Claim 3 (Cancelled).

4. (Previously Presented) A circuit as recited in claim 1, further comprising a time distortion circuit, interposed between the output of the receiver and the input of the transmitter, for introducing predetermined timing distortions into the test signal provided to the receive line of the serial port.

5. (Original) A circuit as recited in claim 1, further comprising a selector, interposed between the output of the receiver and the input of the

transmitter, for selecting between the output of the receiver and a direct input, wherein the direct input provides a predetermined serial bit stream that is different from the test signal received by the receiver.

6. (Original) A circuit as recited in claim 1, wherein the receiver comprises a differential comparator having first and second programmable thresholds.

7. (Original) A circuit as recited in claim 1, wherein the transmitter comprises a differential driver having first and second programmable levels.

8. (Previously Presented) A circuit for testing serial ports in an automatic test system comprising:

a receiver having an input and an output, for receiving a test signal from a transmit line of a serial port;

a transmitter having an input and an output, for transmitting a test signal to a receive line of the serial port, wherein the input of the transmitter is coupled to the output of the receiver for establishing a loopback connection; and

a time distortion circuit, interposed between the output of the receiver and the input of the transmitter, for introducing predetermined timing distortions into the test signal provided to the receive line of the serial port.

9. (Original) A circuit as recited in claim 8, further comprising a time measurement circuit, coupled to the output of the receiver, for measuring timing characteristics of test signals received by the receiver.

Claims 10 and 11 (Cancelled).

12. (Currently Amended) A method of testing a serial port of a device under test in an automatic test system, comprising:

(A) evaluating steady-state characteristics of at least one of a transmit line and a receive line of the serial port;

(B) configuring the device under test to generate a serial bit stream;

(C) measuring at least one timing characteristic of the test signal received with a time measurement circuit;

(D) receiving the serial bit stream from the transmit line of the serial port of the device under test;

(E) transmitting one of the received serial bit stream and a direct input to the receive line of the serial port of the device under test; and

(F) monitoring the device under test to determine whether the serial bit stream received by the device under test matches an expected serial bit stream.

13. (Currently Amended) A method as recited in claim 12, further comprising introducing predetermined timing distortions into the test signal received in step D ~~C~~, prior to transmitting the test signal to the device under test in step ~~D~~ E.

14. (Original) A method as recited in claim 13, wherein the predetermined timing distortions include jitter.

Claim 15 (Cancelled).

16. (Currently Amended) A method as recited in claim 12, wherein the serial bit stream is received in step ~~C~~ D by a comparator having at least one input threshold, and the method further comprises programming the at least one threshold to test whether the device under test produces valid output levels.

17. (Currently Amended) A method as recited in claim 12, wherein the step ~~D~~ E of transmitting includes programming the levels of the transmitted signal to determine whether the device under test responds to input at the programmed levels.

18. (Currently Amended) A method as recited in claim 12, wherein the direct input comprises algorithmic input that is different from the serial bit stream received in step D ~~C~~.

19. (Original) A method as recited in claim 18, wherein the algorithmic input comprises at least one of a pseudo-random sequence of 1's and 0's and an alternating sequence of 1's and 0's.

20. (Previously Presented) A method as recited in claim 12, wherein the direct input conveys a serial bit stream having a frequency that differs from the frequency of the serial bit stream of the transmit line.